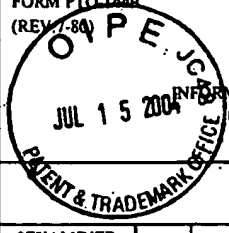
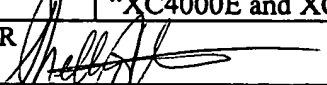


FORM PTO 1448 (REV. 7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. 852463.403		APPLICATION NO. 10/667,199	
 INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)				APPLICANTS Ashish Kumar Goel et al.			
				FILING DATE September 18, 2003		GROUP ART UNIT 2184	
U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION		
					YES	NO	
	AJ						
	AK						
	AL						
	AM						
OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
SAC	AN	ALTERA's Application Note 116 "Configuring APEX 20K, FLEX 10K, FLEX 6000 Devices," pp. 1-77, May 2000.					
SAC	AO	ALTERA's Application Note 33 "Configuring FLEX 8000 devices," pp. 33-71, June 2000.					
SAC	AP	Xilinx's Application Note XAPP138 "Virtex FPGA Series Configuration and Readback," pp. 1-39, July 11, 2002.					
SAC	AQ	Xilinx Inc., <i>The programmable Logic databook 1999</i> , May 14, 1999, version 1.6, "XC4000E and XC4000X Series Field Programmable Gate Arrays," pp. 6-49 - 6-72.					
EXAMINER 				DATE CONSIDERED 1-23-07			
* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).							